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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,688	07/24/2003	Masashi Hiratsuka	116662	9932
25944	7590	05/23/2005	EXAMINER	
OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			STERRETT, JEFFREY L	
			ART UNIT	PAPER NUMBER
			2838	

DATE MAILED: 05/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/625,688

Applicant(s)

HIRATSUKA ET AL.

Examiner

Jeffrey L. Sterrett

Art Unit

2838

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 May 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 15 is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1-5 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Sakakibara et al (US 4,679,129).

Sakakibara et al discloses a power supply (figure 8) comprising first (23a) and second (23b) parallel resonance circuits, first (11) and second (18) transistors respectively connected to the first and second resonance circuits forming first and second parallel resonance circuit parts, and a series resonance circuit (26) having one end connected (via DC source 12) to "an end" of **the first parallel resonance circuit part** and the other end connected (via primary winding n1) to "an end" of **the second parallel resonance circuit part** wherein the first and second parallel resonance circuits are coupled to a DC power supply (collectively 12 and 19) and the first and second transistors are alternatively switched (i.e. out of phase with each other).

3. Claims 6, 7, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakakibara et al.

Sakakibara et al discloses a power supply as explained above and as recited by claims 6, 7, 11, and 12 except for utilizing current limiting resistors. Official notice is taken that current limiting resistors were notoriously old and known expedients in the art at the time of the invention. It would have been obvious to one of ordinary skill in the art at the time of the invention to modified the power supply of Sakakibara et al by utilizing current limiting resistors in order to limit the current through the transistors to a safe or desired level.

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4. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakakibara et al in view of Jacobson et al (US 5,151,852).

Sakakibara et al discloses a power supply as explained above and as recited by claim 8 except for providing the output of the power supply at a node between the capacitor and inductor of the series resonance circuit. Jacobson et al discloses a power supply (12) old and known in the art at the time of the invention where the output of the power supply is provided at a node between the capacitor (C3) and inductor (L5) of the series resonance circuit (20). It would have been obvious to one of ordinary skill in the art at the time of the invention to modified the power supply of Sakakibara et al by providing the output of the power supply at a node between the capacitor and inductor of the series resonance circuit as taught by Jacobson et al in order to derive a desired output waveform.

5. Claims 9 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakakibara et al.

Sakakibara et al discloses a power supply as explained above and as recited by claims 9 and 13 except for utilizing a voltage doubler rectifier circuit. Official notice is taken that voltage doubler rectifier circuits were notoriously old and known expedients in the art at the time of the invention. It would have been obvious to one of ordinary skill in the art at the time of the invention to modified the power supply of Sakakibara et al by utilizing a voltage doubler rectifier circuit on the output of the power supply in order to boost the output voltage to a desired level.

6. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakakibara et al.

Sakakibara et al discloses a power supply as explained above and as recited by claim 14 except for utilizing the power supply to provide power to an image forming apparatus. Official notice is taken that utilizing a power supply to provide power to an image forming apparatus was an notoriously old and known expedient in the art at the time of the invention. It would have been obvious to one of ordinary skill in the art at the time of the invention to utilized the power supply of Sakakibara et al to provide power to an image forming apparatus since all electrical devices require a power supply of some kind.

7. Claim 15 is allowed.

8. Applicant's arguments filed May 4, 2005 have been fully considered but they are not persuasive.

The broad and generic recitation amended into independent claims 1, 10, and 14 that the first and second parallel resonance circuits being coupled to a common DC power supply does not distinguish over the disclosure of Sakakibara et al as explained above. In order to distinguish over the prior art it is recommended that independent claims 1, 10, 14, and 15 be amended to more clearly and distinctly set forth a power supply apparatus as disclosed in figure 2 of the application, i.e. a power supply apparatus comprising first and second parallel resonance circuits each having first and second terminals, first and second switching elements connected to respective second terminals of the first and second parallel resonance circuits, and a series resonance

circuit connected between the second terminals of the first and second parallel resonance circuits, wherein the first terminals of the first and second parallel resonance circuits are connected to a common supply voltage provided by a DC power supply. This recommendation is based on the observation that essentially applicants invention is an "H" circuit wherein the two upper arms are matching parallel resonance circuits, the lower arms are switching elements, and the crossbar is a series resonance circuit (which is weakly set forth at by new claim 15, but could more distinctly be set forth) and the power supply disclosed by Sakakibara et al in figure 8 is essentially a resonant half bridge circuit with two parallel resonant circuits and a series resonant circuit.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

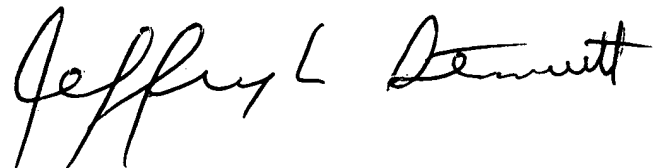
10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey L. Sterrett whose telephone number is (571)

272-2085. The examiner can normally be reached on Monday-Thursday & 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2084. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeffrey L. Sterrett
Primary Examiner
Art Unit 2838

A handwritten signature in black ink, appearing to read "Jeffrey L. Sterrett", written in a cursive style.